

Notice of Allowability	Application No.	Applicant(s)	
	10/043,724	LEE, KANG-YOON	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 8/25/03.
 2. ☒ The allowed claim(s) is/are 1,4-21 and 23-26.
 3. ☒ The drawings filed on 08 January 2002 are accepted by the Examiner.
 4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
- * Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
 - (a) ☐ The translation of the foreign language provisional application has been received.
 6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
8. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No. _____.
 - (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
 - (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the margin according to 37 CFR 1.121(d).

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1 <input type="checkbox"/> Notice of References Cited (PTO-892) | 5 <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 2 <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6 <input checked="" type="checkbox"/> Interview Summary (PTO-413), Paper No. <u>112003</u> |
| 3 <input checked="" type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No. <u>112003</u> | 7 <input checked="" type="checkbox"/> Examiner's Amendment/Comment |
| 4 <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit of Biological Material | 8 <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | 9 <input type="checkbox"/> Other |

DETAILED ACTION

Remarks

1. The objection to claims 1, 3, 7, 9-14, 16, 17, 20-23; 112-second-paragraph rejection to claims 8 and 21; 102(b) rejection and 103(a) rejection are withdrawn.
2. IDS filed 11/20/03 are accepted.
3. Claims 2, 3 and 22 are cancelled. Claims 24-26 are newly added. Thus, claims 1, 4-21 and 23-26 are pending in the application.

Examiner's Amendment

4. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Ho Soon Lee on Nov. 20, 2003.

5. The application has been amended as follows:

In claim 1, add -- **(e)** -- before "forming first conductive type ..." (line 13); add -- **(f)** -- before "thereafter" (line 15); add -- **(g)** -- before "forming a second conductive type ..." (line 17); add -- **(h)** -- before "concurrently....." (line 19); and delete "**and**" after "... by etching the interlayer insulating layer;" (at line 16)

Cancel claim 2.

In claim 7 (line 1) and claim 8 (line 1), replace "wherein (e)" with -- wherein **(h)** --.

In claim 7 (line 2) and claim 8 (line 2), replace “ the conductive material” with -- the **first and second conductive type polysilicon layers** --.

In claim 14 (line 2), delete “**conductive**” before “metal.”

In claim 20 (line 1), delete “**of (c)**” after “opening.”

In claim 21 (line 3), delete “**in the memory cells**” after “data.”

In claim 21 (line 13), add “**first**” before “insulating layer.”

In claim 21, add -- **(f)** -- before “forming a second etch stopping ...” (line 19); replace “(f)” with --**(g)** -- (line 20); and replace “(g)” with -- **(h)** -- (line 22).

In claim 24, add -- **(a)** -- before “forming isolation ..” (line 3); add -- **(b)** -- before “forming a first ...” (line 5); add -- **(c)** -- before “ forming an interlayer ..” (line 9); add-- **(d)** -- before “ etching..” (line 11); add -- **(e)** -- before “ forming first ...” (line 13); add -- **(f)** -- before “ thereafter..” (line 15); add -- **(g)** -- before “ forming a second ..” (line 17); and add -- **(h)** -- before “ etching back ..” (line 19).

In claim 26, replace “ claim 24” with -- claim **25** --.

Allowable Subject Matter

6. Claims 1, 4-21 and 23-26 are allowed.

7. The following is an examiner’s statement of reasons for allowance:

In re claims 1, 9, 16 and 24, the prior art of record, Yoshida et al. (US 5,981,369), teaches a method for forming a semiconductor device on a semiconductor substrate, the method comprising:

(a) forming isolation layers 2 that define a memory cell area (i.e. memory array) and a peripheral circuit area on the semiconductor substrate 1 and isolate each area (Figs.1-2);

(b) forming a first conductive type transistor (n-type transistor) 8A in the memory cell area and a first conductive type transistor (n-type transistor) 8B and a second conductive type transistor (p-type transistor) 8C in the peripheral circuit area, each transistor including source/drain regions 11 for 8A, 12/13 for 8B and 14/15 for 8C, a gate electrode, 8A, 8B and 8C having sidewall spacers 10, and a first etch stopping layer 9 (silicon nitride) (Fig.7);

(c) forming an interlayer insulating layer 16 (silicon oxide) overlying the first and second conductive type transistors 8A-8C (Fig.8);

(d) removing portions of the interlayer insulating layer 16 to form openings (i.e. contact holes) 17-22 that expose the source/drain regions 11, 12/13, 14/15 of the transistors 8A-8C in the memory cell area and the peripheral circuit area (Fig.8), and filling the openings 17-22 with a conductive material TiN/W (Fig.9 and col. 5, lines 56-58); and

(e) concurrently forming contact pads (i.e. plug) 23 on the source/drain regions 11 in the memory cell area and the source/drain regions 12/13 and 14/15 in the peripheral circuit area (Fig.9), i.e. comprises etching back the conductive material (i.e. W/TiN) in the memory cell area and the peripheral circuit area, and etching back the interlayer insulating layer 16 in the memory cell area and the peripheral circuit area; and chemical mechanical polishing the conductive material and the interlayer insulating layer 16 as shown in Fig. 9.

In re claim 21, Yoshida et al. also teach a method of forming a semiconductor device including a memory cell area having a plurality of memory cells and a peripheral circuit area for writing and reading data in the memory cells in the memory cell area of a semiconductor substrate, the method comprising:

- (a) forming isolation layers 2 for defining a memory cell area (i.e. memory array) and a peripheral circuit area on the semiconductor substrate 1 and isolating each area (Figs. 1-2);
- (b) forming a first conductive type transistor (n-type) in the memory cell area and a first conductive type transistor and a second conductive type (p-type) transistor in the peripheral circuit area by forming source/drain regions 11, 12/13 and 14/15 and gate electrodes 8A-8C having sidewall spacers 10, and first etch stopping layers 9 (silicon nitride) in the memory cell area and the peripheral circuit area of the semiconductor substrate (Fig.7);
- (c) forming a first insulating layer 16 overlying the transistors 8A-8C (Fig.8);
- (d) forming plugs (i.e. a layer of tungsten, col.5, lines 56-58) by patterning the insulating layer 16, forming openings 17-22 in the source/drain regions 11, 12/13 and 14/15 of the transistors 8A-8C in the memory cell area and the peripheral circuit area, and filling the openings 17-22 with a conductive material (i.e. tungsten, col.5, lines 56-58);
- (e) forming contact pads (i.e. plug) 23 on the source/drain regions 11 in the memory cell area and the source/drain regions 12/13 and 14/15 in the peripheral circuit area (Fig.9), concurrently by etching the first insulating layer 16 and the plugs and then node-separating the plugs;
- (f) forming a second insulating layer 27 on the contact pads 23 (Fig.12); and
- (g) forming a contact plug 30 on at least one contact pad 23 (Fig.13).

In contrast, in re claims 1 and 24, Yoshida et al., at least neither teach nor suggest forming *first conductive type polysilicon* layers on the exposed source/drain regions of the first conductive type transistor; *thereafter* exposing the source/drain regions of the *second* conductive type transistor in the *peripheral circuit area* by *etching the interlayer insulating* layer; and

forming a *second conductive type polysilicon layer* on the exposed source/drain regions of the second conductive transistor.

In re claim 9, Yoshida et al. neither teach nor suggest forming *conductive epitaxial layers*, which extend from the source/drain regions *onto the isolation layers*, on the respective source/drain regions. In addition, applicant's argument against to secondary reference is persuasive. (see applicant's argument for details).

In re claim 16, Yoshida et al. neither teach nor suggest implanting first and second conductive type impurities *into the opening of the interlayer insulating layer*. In addition, applicant's argument against to secondary reference is persuasive. (see applicant's argument for details).

In re claim 21, the rejection has been overcome by amendment, i.e. Yoshida et al. neither teach nor suggest forming a *second etch stopping layer on the contact pads* and forming a second insulating layer on the contact pads *with the second etch stopping layer*.

8. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone number for the organization where this application or proceeding is assigned is 703-305-3431.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hsien-Ming Lee
Examiner
Art Unit 2823

A handwritten signature in black ink, appearing to read "Hsien-Ming Lee", followed by a long horizontal line.

Nov. 20, 2003